Wujie Wen

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Education

Ph.D. in Computer Engineering, University of Pittsburgh, Pittsburgh, PA, USA, 09/2011-08/2015
Thesis: "Error Characterization and Correction Techniques for Reliable STT-RAM Designs"
Advisor: Prof. Yiran Chen, Duke University

M.S. in Electronic Engineering, Tsinghua University, Beijing, China, 09/2007-07/2010

B.S. in Electronic Engineering (**honor class**), Beijing Jiaotong University, Beijing, China, 09/2002-07/2006

Employment & Professional Experience

Assistant Professor, Department of ECE, Lehigh University, 09/2019-Present

Assistant Professor, Department of ECE, Florida International University, 09/2015-08/2019

Visiting Faculty Research Fellow, Air Force Research Laboratory, 06/2017-08/2017

Intern Engineer, Wireless Connectivity Group, Broadcom Corp., 01/2013-04/2013 & 05/2012-08/2012

ASIC Design Engineer, GPU Design Group, Advanced Micro Devices (AMD) Inc., 07/2010-07/2011

Honors and Awards

- 2020 MICCAI Society Young Scientist Award Nomination and Shortlist for paper–"Orchestrating Medical Image Compression and Remote Segmentation Networks", Lima, Peru (First author by my Ph.D student).
- Best Paper Award Nomination at ASP-DAC, Jeju Island, Korea, Jan. 2018 (Topic–"Deep Learning Security", First author by Ph.D. student–Qi Liu).
- Best Paper Award Nomination at ASP-DAC, Jeju Island, Korea, Jan. 2018 (Topic–"Neuromorphic Computing", First author by Ph.D. student–Tao Liu).
- Best Paper Award Nomination at ICCAD, San Diego, CA, Nov. 2018 (Topic–"Deep Learning Security").
- Best Paper Award Nomination at DATE, Dresden, Germany, Mar. 2016 (First author by me).
- Best Paper Award Nomination at 51th DAC, San Francisco, CA, June 2014 (First author by me).
- Visiting Faculty Research Program Fellowship, Air Force Research Lab, Rome, NY, June 2017.
- Dean's Fellowship, Swanson School of Engineering, University of Pittsburgh, 2015.
- Best Ph.D. Forum Poster Presentation at DAC, San Francisco, CA, June 2015.
- John A. Jurenko Graduate Fellowship, University of Pittsburgh, 2013.
- ACM Special Interest Group on Design Automation (SIGDA) Student Research Competition (SRC) Bronze medal, ICCAD, San Jose, CA, Nov. 2014.
- 49th Design Automation Conference (DAC) A. Richard Newton Graduate Scholarship ($24,000), the only awardee for outstanding research in EDA Domain, San Francisco, CA, June 2012.
- DAC Young Student Support Program Award, June 2012.

Publications

Conference Publications: DAC(13)/ICCAD(10)/HPCA, HOST/ACSAC, CVPR/AAAI/ECCV etc.

60. **ACSAC2020**: T. Liu[D], Z. Liu[D], Q. Liu[D], **W. Wen**, W. Xu and M. Li, "StegoNet: Turn Deep Neural Network into a Stegomalware", Proc. ACM 36th Annual Computer Security Application Conference **(ACSAC)**, Austin, TX, Dec. 2020, to appear. (Acceptance Rate: 70/302=23%)

59. **ICCAD2020**: Q. Liu[D], **W. Wen** and Y. Wang, "Concurrent Weight Encoding-based Detection for Bit-Flip Attack on Neural Network Architecture", Proc. ACM/IEEE 39th International Conference on Computer-Aided Design **(ICCAD)**, pp. 1–8, Nov. 2020, to appear.

58. **ICCAD2020**: C. Zhang, K. Abdelaal, A. Chen, X. Zhao, **W. Wen** and X. Guo, "ECC Cache: A Lightweight Error Detection for Phase-Change Memory Stuck at Faults", Proc. ACM/IEEE 39th International Conference on Computer-Aided Design **(ICCAD)**, pp. 1–9, Nov. 2020, to appear.

57. **ECCV2020**: X. Ma, W. Niu, T. Zhang, S. Liu, S. Lin, H. Li, **W. Wen**, X. Chen, J. Tang, K. Ma, B. Ren, and Y. Wang, "An Image Enhancing Pattern-based Sparsity for Real-time Inference on Mobile Devices", Proc. of the 16th European Conference on Computer Vision **(ECCV)**, Sep. 2020, pp. 1-16. (Acceptance Rate: 1361/5025=27%)

56. **MICCAI2020**: Q. Liu[D], H. Jiang[D], T. Liu[D], Z. Liu[D], S. Li, **W. Wen** and Y. Shi, "Defending Deep Learning-based Biomedical Image Segmentation from Adversarial Attacks: A Low-cost Frequency Refinement Approach", the 23rd International Conference on Medical Image Computing and Computer Assisted Intervention **(MICCAI)**, Lima, Peru, Oct 2020, pp. 1-9. (Early Accept)

55. **MICCAI2020**: Z. Liu[D], S. Li, Y. Chen, T. Liu[D], Q. Liu[D], X. Xu, Y. Shi, and **W. Wen**, "Orchestrating Medical Image Compression and Remote Segmentation Networks", the 23rd International Conference on Medical Image Computing and Computer Assisted Intervention **(MICCAI)**, Lima, Peru, Oct 2020, pp. 1-10. (Early Accept)

54. **DAC2020**: N. Xu[D], Q. Liu[D], T. Liu[D], Z. Liu[D], X. Guo and **W. Wen**, "Stealing Your Data from Compressed Machine Learning Models", Proc. ACM/IEEE 57th Design Automation Conference **(DAC)**, San Francisco, CA, 2020, pp. 1-6. (Acceptance Rate: 228/991=23.0%)

53. **DAC2020**: Q. Liu[D], T. Liu[D], Z. Liu[D], **W. Wen** and C. Yang, "Monitoring the Health of Emerging Neural Network Accelerators with Cost-effective Concurrent Test", Proc. ACM/IEEE 57th Design Automation Conference **(DAC)**, San Francisco, CA, 2020, pp. 1-6. (Acceptance Rate: 228/991=23.0%)

52. **ASPDAC2020**: X. Ma, G. Yuan, S. Lin, C. Ding, F. Yu, T. Liu[D], **W. Wen**, X. Chen and Y. Wang, "Tiny but Accurate: A Pruned, Quantized and Optimized Memristor Crossbar Framework for Ultra Efficient DNN Implementation," Proc. ACM/IEEE 25th Asia and South Pacific Design Automation Conference (ASP-DAC 2020), Jan. 2020, pp. 301-306. (Acceptance Rate: 86/279=30%)

51. **ICCAD2019**: T. Liu[D] and **W. Wen**, "Making the Fault-Tolerance of Emerging Neural Network Accelerators Scalable", Proc. ACM/IEEE 38th International Conference on Computer-Aided Design **(ICCAD)**, Nov. 2019, pp. 1-5. (Invited Tutorial)

50. **CVPR2019**: Z. Liu[D], X. Xu, T. Liu[D], Q. Liu[D], Y. Wang, Y. Shi, **W. Wen**, M. Huang, H. Yuan and J. Zhuang, "Machine Vision Guided 3D Medical Image Compression for Efficient Transmission and Accurate Segmentation in the Clouds," IEEE Computer Society Conference on Computer Vision and Pattern Recognition (**CVPR**), Long Beach, CA, 2019, pp. 12687-12696.

49. **CVPR2019**: Z. Liu[D], T. Liu[D], Q. Liu[D], N. Xu[D], X. Lin, Y. Wang and **W. Wen**, "Feature Distillation: DNN-Oriented JPEG Compression Against Adversarial Examples," IEEE Computer Society Conference on Computer Vision and Pattern Recognition (**CVPR**), Long Beach, CA, 2019, pp. 860-868.

48. **DAC2019**: T. Liu[D], **W. Wen**, L. Jiang, Y. Wang, C. Yang and G. Quan, "A Fault-Tolerant Neural Network Architecture", Proc. ACM/IEEE Design Automation Conference **(DAC)**, Las Vegas, NV, 2019, pp. 1-6. (Acceptance Rate: 202/815=24.8%)

47. **HPCA2019**: Z. Li, C. Ding, S. Wang, **W. Wen**, Y. Zhuo, C. Liu, Q. Qiu, W. Xu, X. Lin, X. Qian, Y. Wang, "E-RNN: Design Optimization for Efficient Recurrent Neural Networks in FPGAs," Proc. of the 25th International Symposium on High-Performance Computer Architecture **(HPCA)**, Feb. 2019, pp. 69-80. (Acceptance Rate: 46/233=19.7%)

46. **CCGRID2019**: S. Homsi, G. Quan, **W. Wen**, G. A. Chapparo-Baquero and L. Njilla, "Game Theoretic-Based Approaches for Cybersecurity-Aware Virtual Machine Placement in Public Cloud Clusters", the 19th IEEE/ACM International Symposium on Cluster, Cloud and Grid Computing **(CCGRID)**, May 2019, pp. 272-281. (Acceptance Rate: 47/207=22.7%)

45. **AAAI2019**: Y. Wang, Z. Zhan, J. Tang, B. Yuan, L. Zhao, **W. Wen**, S. Wang, and X. Lin, "Universal Approximation Property and Equivalence of Stochastic Computing-based Neural Networks and Binary Neural Networks, Proc. of the 33rd AAAI Conference on Artificial Intelligence **(AAAI)**, Feb. 2019, pp. 5369-5376. (Acceptance Rate: 1150/7095=16.2%).

44. **WiSec2019**: T. Liu[D] and **W. Wen**, "Deep-evasion: Turn deep neural network into evasive self-contained cyber-physical malware: poster", Proceedings of the 12th Conference on Security and Privacy in Wireless and Mobile Networks (WiSec), May 2019, pp. 320-321.

43. **ASP-DAC2019**: T. Liu[D], N. Xu[D], Q. Liu[D], Y. Wang, and **W. Wen**, "A System-level Perspective to Understand the Vulnerability of Deep Learning Systems," Proc. ACM/IEEE 23rd Asia and South Pacific Design Automation Conference (ASP-DAC), Jan. 2019, pp. 506-511. (Invited Special Session)

42. **ICCAD2018**: S. Wang, X. Wang, P. Zhao, **W. Wen**, D. Kaeli, P. Chin, and X. Lin, "Defensive dropout for hardening deep neural networks under adversarial attacks," IEEE/ACM International Conference On Computer Aided Design **(ICCAD)**, Nov. 2018, pp. 71:1-71:8. (**Best Paper Award Nomination**, Acceptance Rate: 98/396=25%)

41. **ICCAD2018**: Q. Lou, **W. Wen**, and L. Jiang, "3DICT: A Reliable and QoS Capable Mobile Process-In-Memory Architecture for Lookup-based CNNs in 3D XPoint ReRAMs," IEEE/ACM International Conference On Computer Aided Design **(ICCAD)**, Nov. 2018, pp. 53:1-53:8. (**Best Paper Award Nomination** from track–Hardware for Embedded Systems, Acceptance Rate: 98/396=25%)

40. **ECCV2018**: T. Zhang, S. Ye, K. Zhang, J. Tang, **W. Wen**, M. Fardad, Y. Wang, "A Systematic DNN Weight Pruning Framework using Alternating Direction Method of Multipliers," Proc. of the 15th European Conference on Computer Vision **(ECCV)**, Sep. 2018, pp. 1-16. (Acceptance Rate: 717/2439=29%)

39. **DAC2018**: Z. Liu[D], T. Liu[D], **W. Wen**, L. Jiang, J. Xu, Y. Wang and G. Quan, "DeepN-JPEG: A Deep Neural Network Favorable JPEG-based Image Compression Framework," Proc. ACM/IEEE Design Automation Conference **(DAC)**, June 2018, pp. 1-6. (Acceptance Rate: 168/691=24.3%)

38. **HOST2018**: T. Liu[D], **W. Wen** and Y. Jin, "SIN^2: Stealth Infection on Neural Network–A Low-cost Agile Neural Trojan Attack Methodology," Proc. IEEE International Symposium on Hardware Oriented Security and Trust **(HOST)**, Washington, DC, May 2018, pp. 227-230. (Acceptance Rate: 22/84=26.2%)

37. **ASP-DAC2018**: Q. Liu[D],, T. Liu[D], Z. Liu[D], Y. Wang, Y. Jin and **W. Wen**, "Security Analysis and Enhancement of Model Compressed Deep Learning Systems under Adversarial Attacks," Proc. ACM/IEEE 23rd Asia and South Pacific Design Automation Conference (ASP-DAC), Jan. 2018, pp. 721-726. **(Best Paper Award Nomination)**

36. **ASP-DAC2018**: T. Liu[D], L. Jiang, Y. Jin, G. Quan and **W. Wen**, "PT-Spike: A Precise-Time-Dependent Single Spike Neuromorphic Architecture with Efficient Supervised Learning," Proc. ACM/IEEE 23rd Asia and South Pacific Design Automation Conference (ASP-DAC), Jan. 2018, pp. 568-573. **(Best Paper Award Nomination)**

35. **ISVLSI2018**: Z. Liu[D], T. Liu[D], J. Guo, N. Wu and **W. Wen**, "An ECC-Free MLC STT-RAM Based Approximate Memory Design for Multimedia Applications," Proc. IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Jul. 2018, pp. 142-147. (Oral Acceptance Rate: 57/192=29%)

34. **ISVLSI2018**: T. Liu[D], Z. Liu[D], Q. Liu[D] and **W. Wen**, "Enhancing the Robustness of Deep Neural Networks from "Smart" Compression," Proc. IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Jul. 2018, pp. 528-532. (Invited Special Session)

33. **ICC2018**: H. Wu, L. Chen, C. Shen, **W. Wen** and J. Xu, "Online Geographical Load Balancing for Energy-Harvesting Mobile Edge Computing," IEEE International Conference on Communications (ICC) 2018 Green Communications Systems and Networks Symposium, May. 2018, pp. 1-6.

32. **ICCAD2017**: T. Liu[D], Z. Liu[D], F. Lin, Y. Jin, G. Quan, and **W. Wen**, "MT-Spike: A Multilayer Time-based Spiking Neuromorphic Architecture with Temporal Error Backpropagation," Proc. ACM/IEEE International Conference on Computer-Aided Design **(ICCAD)**, Nov. 2017, pp. 1-8. **(Best Paper Award Nomination from track–Hardware for Embedded Systems)**

31. **DATE2016**: **W. Wen**, M. Mao, H. Li, Y. Chen[DA], Y. Pei and N. Ge, "A Holistic Tri-region MLC STT-RAM Design with Combined Performance, Energy, and Reliability Optimizations," Proc. ACM/IEEE Design, Automation & Test in Europe **(DATE)**, Mar. 2016, pp. 1285-1290. **(Best Paper Award Nomination, 13 out of 829, top 1.5%)**

30. **ISLPED2017**: L. Jiang, M. Kim, **W. Wen**, and D. Wang, "XNOR-POP: A Processing-in-Memory Architecture for Binary Convolutional Neural Networks in Wide-IO2 DRAMs," Proc. ACM/IEEE International Symposium on Low Power Electronics and Design **(ISLPED)**, Aug. 2017, pp. 1-6. (Acceptance Rate: 24%)

29. **ASP-DAC2017**: Z. Liu[D], **W. Wen**, L. Jiang, Y. Jin, and G. Quan, "A Statistical STT-RAM Retention Model for Fast Memory Subsystem Designs," Proc. ACM/IEEE 21th Asia and South Pacific Design Automation Conference (ASP-DAC), Jan. 2017, pp. 720-725. (Acceptance rate: 111/358 = 31%)

28. **ASP-DAC2017**: X. Yang and **W. Wen**, "Design of A Pre-scheduled Data Bus (DBUS) for Advanced Encryption Standard (AES) Encrypted System-on-Chips (SoCs)," Proc. ACM/IEEE 21th Asia and South Pacific Design Automation Conference (ASP-DAC), Jan. 2017, pp. 506-511. (Acceptance rate: 111/358 = 31%)

27. **ASP-DAC2017**: A. Ren, S. Liu, R. Cai, **W. Wen**, P. Varshney and Y. Wang, "Algorithm-Hardware Co-optimization of Memristor-Based Framework for Solving SOCP and Homogeneous QCQP Problems," Proc. ACM/IEEE 21th Asia and South Pacific Design Automation Conference (ASP-DAC), Jan. 2017, pp. 788-793. (Acceptance rate: 111/358 = 31%)

26. **GLSVLSI2017**: L. Jiang, S. Mittal, and **W. Wen**, "Building a Fast and Power Efficient Inductive Charge Pump System for 3D Stacked Phase Change Memories," Proc. ACM Great Lakes Symposium on VLSI (GLSVLSI), May 2017, pp. 275-280.

25. **GLSVLSI2017**: S. Sha, **W. Wen**, S. Ren and G. Quan, "A Thermal-Balanced Variable-Sized-Bin-Packing Approach for Energy Efficient Multi-Core Real-Time Scheduling," Proc. ACM Great Lakes Symposium on VLSI (GLSVLSI), May 2017, pp. 257-262.

24. **ISQED2017**: T. Liu[D], and **W. Wen**, "A Fast and Ultra Low Power Time-Based Spiking Neuromorphic Architecture for Embedded Applications," Proc. IEEE 18th International Symposium on Quality Electronic Design (ISQED), Mar. 2017, pp. 19-22. (Invited Special Session)

23. **ISQED2017**: G. Chaparro-Baquero, S. Sha, S. Homsi, **W. Wen** and G. Quan, "Processor/Memory Co-scheduling Using Periodic Resource Server for Real-Time System Under Peak Temperature Constraints," Proc. IEEE 18th International Symposium on Quality Electronic Design (ISQED), Mar. 2017, pp. 360-366.

22. **ICCAD2016**: C. Yang, B. Liu, **W. Wen**, M. Barnell, Q. Wu, H. Li, Y. Chen[DA] and J. Rajendran, "Security of Neuromorphic Computing: Thwarting Learning Attacks Using Memristor's Obsolescence Effect," Proc. ACM/IEEE International Conference on Computer Aided Design **(ICCAD)**, Nov. 2016, pp. 1-6. (Acceptance rate: 97/408 = 24%)

21. **ICCAD2016**: S. Li, **W. Wen**, Y. Wang, Q. Qiu, Y. Chen[DA] and H. Li, "A Data Locality-aware Design Framework for Reconfigurable Sparse Matrix-Vector Multiplication Kernel," Proc. ACM/IEEE International Conference on Computer Aided Design **(ICCAD)**, Nov. 2016, pp. 1-6. (Acceptance rate: 97/408 = 24%)

20. **ICPP2016**: S. Sha, **W. Wen**, M. Fan, S. Ren and G. Quan, "Performance Maximization via Frequency Oscillation on Temperature Constrained Multicore Processors," Proc. ACM/IEEE International Conference on Parallel Processing (ICPP), Aug. 2016, pp. 526-535. (Acceptance rate: 53/251 = 21.1%)

19. **DAC2016**: X. Chen, N. Khoshavi, J. Zhou, D. Huang, R. DeMara, J. Wang, **W. Wen** and Y. Chen[DA],"AOS: Adaptive Overwrite Scheme for Energy-Efficient MLC STT-RAM Cache," Proc. ACM/IEEE Design Automation Conference **(DAC)**, Jun. 2016, pp. 1-6. (Acceptance rate: 152/878 = 17.3%)

18. **DAC2016**: T. W, Q. Han, S. Sha, **W. Wen**, G. Quan and M. Qiu "On Harmonic Fixed-Priority Scheduling of Periodic Real-Time Tasks with Constrained Deadlines," Proc. ACM/IEEE Design Automation Conference **(DAC)**, Jun. 2016, pp. 1-6. (Acceptance rate: 152/878 = 17.3%)

17. **DAC2016**: E. Eken, L. Song, I. Bayram, C. Xu, **W. Wen**, Y. Xie and Y. Chen[DA], "NVSim-VXs: An Improved NVSim for Variation Aware STT-RAM Simulation," Proc. ACM/IEEE Design Automation Conference (DAC), Jun. 2016, pp. 1-6. (Acceptance rate: 152/878 = 17.3%)

16. **DAC2016**: M. Mao, **W. Wen**, X. Liu, J. Hu, D. Wang, Y. Chen and H. Li, "TEMP: Thread Batch Enabled Memory Partitioning for GPU," Proc. ACM/IEEE Design Automation Conference **(DAC)**, Jun. 2016, pp. 1-6. (Acceptance rate: 152/878 = 17.3%)

15. **DATE2016**: X. Wang, M. Mao, E. Eken, **W. Wen**, H. Li and Y. Chen[DA], "Sliding Basket: An Adaptive ECC Scheme for Runtime Write Failure Suppression of STT-RAM Cache," Proc. ACM/IEEE Design, Automation & Test in Europe **(DATE)**, Mar. 2016, pp.762-767. (Acceptance rate: 199/824 = 24.0%).

14. **ASP-DAC2016**: L. Jiang, **W. Wen**, D. Wang and L. Duan, "Improving Read Performance of STT-MRAM based Main Memories through Smash Read and Flexible Read," Proc. ACM/IEEE 21th Asia and South Pacific Design Automation Conference (ASP-DAC), Jan. 2016, pp.31-36. (Acceptance rate: 94/274 = 34.3%)

13. **ASP-DAC2016**: X. Zhang, G. Sun, Y. Zhang, **W. Wen**, Y. Chen[DA], H. Li, "A Novel PUF based on Cell Error Rate Distribution of STT-RAM," Proc. ACM/IEEE 21th Asia and South Pacific Design Automation Conference (ASP-DAC), Jan. 2016, pp.342-347. (Acceptance rate: 94/274 = 34.3%)

12. **ISVLSI2016**: K. Shamsi, Y. Jin and **W. Wen**, "Hardware Security Challenges Beyond CMOS: Attacks and Remedies," Proc. IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Jul. 2016, pp. 200-205 (Invited Special Session).

11. **ISVLSI2016**: B. Li, Y. Pei and **W. Wen**, "Efficient Low-Density Parity-Check (LDPC) Code Decoding for Combating Asymmetric Errors in STT-RAM," Proc. IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Jul. 2016, pp. 266-271.

10. **DAC2015**: J. Guo, **W. Wen**, J. Hu, D. Wang, H. Li and Y. Chen, "FlexLevel: a Novel NAND Flash Storage System Design for LDPC Latency Reduction," Proc. ACM/IEEE Design Automation Conference **(DAC)**, Jun. 2015, pp. 1-6. (Acceptance rate: 162/789=20.5%)

9. **DAC2014**: **W. Wen**, Y. Zhang, M. Mao and Y. Chen, "State-Restrict MLC STT-RAM Designs for High-Reliable High-Performance Memory System," Proc. ACM/IEEE Design Automation Conference (DAC), Jun. 2014, pp. 1-6. **(Best Paper Award Nomination, 7 out of 787, 0.9%)**

8. **DAC2014**: M. Mao, **W. Wen**, Y. Zhang, H. Li and Y. Chen, "Exploration of GPGPU Register File Architecture Using Domain-wall-shift-write based Racetrack Memory," Proc. ACM/IEEE Design Automation Conference **(DAC)**, Jun. 2014, pp. 1-6. (Acceptance rate: 174/787 = 22.1%)

7. **DAC2014**: E. Eken, Y. Zhang, **W. Wen**, R. Joshi, H. Li and Y. Chen, "A New Field-Assisted Access Scheme of STT-RAM with Self-Reference Capability,", Design Automation Conference **(DAC)**, Jun. 2014, pp. 1-6. (Acceptance rate: 174/787 = 22.1%)

6. **ISCE2014**: **W. Wen**, Y. Zhang, M. Mao and Y. Chen, "STT-RAM Reliability Enhancement through ECC and Access Scheme Optimization", International Symposium on Consumer Electronics, Jun. 2014, pp. 1-2.

5. **ICCAD2013**: **W. Wen**, M. Mao, X. Zhu, S. Kang, D. Wang and Y. Chen, "CD-ECC: Content-Dependent Error Correction Codes for Combating Asymmetric Nonvolatile Memory Operation Errors," Proc. ACM/IEEE International Conference on Computer Aided Design **(ICCAD)**, Nov. 2013, pp. 1-8. (Acceptance rate: 92/354 = 26%)

4. **DAC2012**: **W. Wen**, Y. Zhang, Y. Chen, Y. Wang and Y. Xie, "PS3-RAM: A Fast Portable and Scalable Statistical STT-RAM Reliability Analysis Method," Proc. ACM/IEEE Design Automation Conference **(DAC)**, Jun. 2012, pp. 1191-1196. (Acceptance rate: 168/741 = 23%)

3. **DATE2013**: J. Guo, **W. Wen**, and Y. Chen, "DA-RAID-5: A Disturb Aware Data Protection Technique for NAND Flash Storage Systems," Proc. ACM/IEEE Design, Automation & Test in Europe **(DATE)**, Mar. 2013, pp. 380-385. (Acceptance rate: 92/354 = 26.0%)

2. **ASP-DAC2013**: **W. Wen**, Y. Zhang, L. Zhang and Y. Chen, "Loadsa: A Yield-Driven Top-Down Design Method for STT-RAM Array," Proc. ACM/IEEE 18th Asia and South Pacific Design Automation Conference (ASP-DAC), Jan. 2013, pp. 291-296. (Acceptance rate ∼31.2%)

1. **ICCAD2012**: Y. Zhang, L. Zhang, **W. Wen**, G. Sun and Y. Chen, "Multi-level Cell STT-RAM: Is It Realistic or Just a Dream?" Proc. ACM/IEEE International Conference on Computer Aided Design **(ICCAD)**, Nov. 2012, pp. 526-532. (Acceptance rate: 82/338 = 24.3%)

Referred Journal Publications:

19. **TODES2020**: S. Sha, A. Bankar, **W. Wen** and G. Quan, "On Fundamental Principles for Thermal-Aware Design on Periodic Real-Time Multi-Core Systems, ACM Transactions on Design Automation of Electronic Systems (TODAES), 2020, vol. 25, no. 2, pp. 23:1–23:23.

18. **TCAD2020**: C. Yang, B. Liu, H. Li, Y. Chen^{DA}, M. Barnell, Q. Wu, **W. Wen** and J. Rajendran, "Thwarting Replication Attack against Memristor-based Neuromorphic Computing System," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Oct. 2020, vol. 39, no. 10, pp. 2192-2205.

17. **CCF-Trans2020**: T. Liu^{D}, G. Quan and **W. Wen**, "FPT-spike: a Flexible Precise-time-dependent Single-spike Neuromorphic Computing Architecture", CCF Transactions on High Performance Computing (HPC), June 2020, pp. 1-16.

16. **JETC2019**: B. Li, M. Mao, X. Liu, T. Liu^{D}, Z. Liu^{D}, **W. Wen**, Y. Chen^{DA} and H. Li, "Thread Batching for High-performance Energy-efficient GPU Memory Design", ACM Journal on Emerging Technologies in Computing Systems (JETC), Dec. 2019, vol. 15, no. 4, pp. 39:1-39:21.

15. **PARCO2019**: S. Sha, **W. Wen**, G. Chaparro-Baquero and G. Quan, "Thermal-Constrained Energy Efficient Real-Time Scheduling on Multi-Core Platforms," Parallel Computing (PARCO), vol. 85, 2019, pp. 231-242, ISSN 0167-8191, https://doi.org/10.1016/j.parco.2019.01.003.

14. **TPDS2018**: S. Sha, **W. Wen**, S. Ren and G. Quan, "M-Oscillating: Performance Maximization on Temperature-Constrained Multi-Core Processors," IEEE Transactions on Parallel and Distributed Systems (TPDS), Nov. 2018, vol. 29, no. 11, pp. 2528-2539.

13. **TCAD2018**: Z. Liu^{D}, M. Mao, T. Liu^{D}, X. Wang, **W. Wen**, Y. Chen^{DA}, H. Li, D. Wang, Y. Pei and N. Ge, "TriZone: A Design of MLC STT-RAM Cache for Combined Performance, Energy, and Reliability Optimizations," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Oct. 2018, vol. 37, no. 10, pp. 1985-1998.

12. **JETC2018**: B. Li, Y. Pei and **W. Wen**, "Efficient LDPC Code Design for Combating Asymmetric Errors in STT-RAM," ACM Journal on Emerging Technologies in Computing Systems (JETC), Mar. 2018, vol. 14, no. 1, pp. 10:1-10:20.

11. **TC2017**: M. Mao, **W. Wen**, Y. Zhang, Y. Chen[DA] and H. Li, "An Energy-Efficient GPGPU Register File Architecture Using Racetrack Memory," IEEE Transactions on Computers (TC), Apr. 2017, vol. 66, no. 9, pp. 1478-1490.

10. **JETC2017**: X. Yang, **W. Wen** and F. Ming, "Improving AES Core Performance via An Advanced ASBUS Protocol," ACM Journal on Emerging Technologies in Computing Systems (JETC), Dec. 2017, vol. 14, no. 1, pp. 6:1-6:23.

9. **TC2016**: X. Chen, N. Khoshavi, R. DeMara, J. Wang, J. Zhou, D. Huang, **W. Wen**, Y. Chen[D], "Energy-Aware Adaptive Restore Schemes for MLC STT-RAM Cache," IEEE Transactions on Computers (TC), Nov. 2016, vol. 66, no. 5, pp. 786-798. **(Feature Paper of Month–May, 2017)**

8. **TCAD2016**: J. Guo, **W. Wen**, J. Hu, D. Wang, H. Li and Y. Chen[DA], "FlexLevel NAND Flash Storage System Design to Reduce LDPC Latency," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Oct. 2016, vol. 36, no. 7, pp. 1167-1180.

7. **TCAD2014**: **W. Wen**, Y. Zhang, Y. Chen, Y. Wang and Y. Xie, "PS3-RAM: A Fast Portable and Scalable Statistical STT-RAM Reliability/Energy Analysis Method," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Nov. 2014, vol. 33, no. 11, pp. 1644-1656.

6. **TMAG2014**: E. Eken, Y. Zhang, **W. Wen**, R. Joshi, H. Li, and Y. Chen, "A Novel Self-reference Technique for STT-RAM Read and Write Reliability Enhancement," IEEE Transaction on Magnetics (TMAG), Nov. 2014, vol. 50, no. 11, 3401404.

5. **TMAG2012**: Y. Zhang, **W. Wen**, and Y. Chen, "The Prospect of STT-RAM Scaling from Read ability Perspective," IEEE Transaction on Magnetics **TMAG**, vol. 48, no. 1, Nov. 2012, pp. 3035-3038.

4. **SPIN2013**: Y. Zhang, **W. Wen**, and Y. Chen, "STT-RAM Cell Design Considering MTJ Asymmetric Switching," SPIN, vol. 2, no. 3, Nov. 2013, 1240007.

3. **JETC2013**: Y. Chen, W. Wong, H. Li, C.-K. Koh, Y. Zhang, and **W. Wen**, "On-chip Caches built on Multi-Level Spin-Transfer Torque RAM Cells and Its Optimizations," ACM Journal on Emerging Technologies in Computing Systems (JETC), vol. 9, no 2, article 16, May 2013.

2. **IET2011**: C. Geng, Y. Pei, **W. Wen**, Z. Luan, N. Ge, "ASIC implementation of fractionally spaced Rake receiver for high data rate UWB," IET Electronic Letters, vol. 47, no. 3, 2011, pp. 215-217.

1. **W. Wen**, Y. Pei and N. Ge, "ASIC design optimization of a decision feedback equalizer at Single-Carrier Ultra-wideband," Journal of Tsinghua University (Science and Technology), vol. 50, no. 4, 2010, pp. 577-580.

Book Chapters:

1. Y. Zhang, **W. Wen**, and Y. Chen[DA], "Asymmetry in STT-RAM Cell Operations," (in Emerging Memory Technologies: Design, Architecture, and Applications, Editor: Yuan Xie), Springer, Aug. 31, 2013, ISBN: 978-14-419-9550-6.

2. **W. Wen**, Y. Zhang, and Y. Chen[DA], "Statistical Reliability/Energy Characterization in STT-RAM Cell Designs," (in Spintronics Based Computing, Editors: Weisheng Zhao and Guillaume Prenat), Springer, Jun. 14, 2015. ISBN:978-3-319-15179-3.

3. Y. Zhang, **W. Wen**, H. Li, and Y. Chen[DA], "The Prospect of STT-RAM Scaling, (in Metallic Spintronic Devices," Editor: Xiaobin Wang), CRC Press, Aug. 4, 2014. ISBN: 978-14-665-8844-8.

Patents Granted

- **W. Wen**, E. Eken, H. Li, X. Bi, and Y. Chen[DA], "Spin-transfer Torque Memory Magnetic-assisted Nondestructive Self-reference Sensing Method," US Provisional Patent Application (US9627024 B2), Apr 18, 2017.

Research Grants

Competitively Awarded Research Grants

1. **National Science Foundation**, Wujie Wen (Lead-PI, Share $355,475), *"SPX: Collaborative Research: Scalable Neural Network Paradigms to Address Variability in Emerging Device based Platforms for Large Scale Neuromorphic Computing"*, SPX-2006748, 11/26/2019-09/30/2023, Total amount: $699,617 ($715,617 with REU Supplemental).

2. **National Science Foundation**, Wujie Wen (PI, Share $235,000), *"SHF: Small: Collaborative Research: Retraining-free Concurrent Test and Diagnosis in Emerging Neural Network Accelerators"*, CCF-2011236, 10/05/2019-09/30/2022, Total amount: $499,998.

3. **National Science Foundation**, Wujie Wen (Single PI, Lehigh), *"EAGER: Invisible Shield: Can Compression Harden Deep Neural Networks Universally Against Adversarial Attacks?"*, SaTC-2011260, 09/01/2018-08/31/2021, Total amount: $250,000.

4. **The Florida Center for Cybersecurity (FC^2)**, Wujie Wen (PI share 50%), *"Towards Robust Deep Learning Systems Against Adversarial Attacks"*, 07/01/2019-06/30/2020, Total amount: $75,000.

5. **The Florida Center for Cybersecurity (FC^2)**, Wujie Wen (PI share 50%), *"Helmet: Deep Neural Network Protection Against Adversarial Attacks"*, 07/01/2017-12/31/2018, Total amount: $50,000.

6. **Air Force Research Lab (AFRL)**, Wujie Wen (PI), *"Security Analysis of Model Compressed Deep Neural Networks Under Adversarial Attacks,"*, 09/15/2017-11/15/2017, $10,000.

7. **Lehigh Collaborative Research Opportunity (CORE) Grant Program**, *"Privacy Implications of Hardware Functionality in Deep Learning"*, Parv Venkitasubramaniam (PI, Share 50%), Wujie Wen (Co-PI, Share 50%), 09/01/2020-08/31/2020, $60,000.

Other Awarded Grants

- **Xilinx University Program Donation**, *"Hardware-software Co-design for Enhancing the Performance and Robustness of Deep Compressed Neural Networks"*, PI, 03/07/2017-03/06/2018, $2,495.

Scholarly Presentations Since 08/2015

1. "A New Path Towards Efficient, Sustainable and Secure Deep Learning System Design", Duke University, Oct. 2019. (Guest Lecture)

2. "Understanding Adversarial Attack and Defense towards Deep Compressed Neural Networks", SPIE2018, Orlando, FL, May 2018.
3. "Beyond Adversarial Attacks: A System-level Perspective to Understand the Vulnerability of Deep Learning Systems", University of Delaware, Apr. 2018. (ECE Spring Seminar Series)
4. "Exploiting Deep Learning System-level Vulnerabilities from the Intelligent Supply Chain", IEEE VLSI Test Symposium, San Francisco, CA, Apr. 2018. (Special Session Invited Talk)
5. "Security Analysis and Enhancement of Model Compressed Deep Learning Systems under Adversarial Attacks", AFRL/RIB, Rome, NY, Aug. 2017.
6. "Building a Fast and Power Efficient Inductive Charge Pump System for 3D Stacked Phase Change Memories", GLSVLSI, Banff, Alberta, Canada, May 2017.
7. "A Fast and Ultra Low Power Time-Based Spiking Neuromorphic Architecture for Embedded Applications," ISQED, Santa Clara, CA, Mar. 2017.
8. "A Statistical STT-RAM Retention Model for Fast Memory Subsystem Designs," ASP-DAC, Chiba, Tokyo, Japan, Jan. 2017.
9. "Design of A Pre-scheduled Data Bus (DBUS) for Advanced Encryption Standard (AES) Encrypted System-on-Chips (SoCs)," ASP-DAC, Chiba, Tokyo, Japan, Jan. 2017.
10. "Hardware Security Challenges Beyond CMOS: Attacks and Remedies," ISVLSI, Pittsburgh, PA, July 2016. (Special Session Organizer)
11. "Robust Cross-layer Designs and Applications of Emerging Memories," University of Science and Technology Beijing, Beijing China, Jun. 2016.
12. "Robust Cross-layer Designs and Applications of Emerging Memories," Tsinghua University, Beijing China, Jun. 2016.
13. "TEMP: Thread Batch Enabled Memory Partitioning for GPU," Design Automation Conference, Austin, TX, Jun. 2016.
14. "RENO: A High-efficient Reconfigurable Neuromorphic Computing Accelerator Design," Pittsburgh, PA, Nov. 2015.

Teaching & Research Advising

Courses

- ECE450-12 "Software-Hardware Co-design of Deep Learning Systems", Fall 2019/Fall 2020, Lehigh University (new course created by me).
- ECE350/450 "Computer-Aided Design of Digital Systems", Spring 2020, Lehigh University (new course created by me).
- EEL6167 "VLSI Design", Fall 2015/2016/2017/2018, FIU.
- EEL6726 "Advanced VLSI Design", Spring 2016/2017/2018/2019, FIU.
- EEL3712 "Logic Design", Fall 2017/2018, Spring 2018/2019, FIU.

Research Advising

Ph.D/Master Students

- Qi Liu, *Ph.D. at Lehigh ECE*, Since 09/2019, Topic: "Deep Learning Security and its Application in EDA", Expected Graduate Date: 08/2023.

- Nuo Xu, *Ph.D. at Lehigh ECE*, Since 09/2019, Topic: "Enhancing the Privacy and Hardware Performance of Deep Learning Systems", Expected Graduate Date: 08/2023.

- Ruoyu Wang, *Ph.D. at Lehigh ECE*, Since 09/2020, Topic: "Software-Hardware Co-Design of Graph Neural Network Acceleration";

- Chaoqi Wang, *Ph.D. at Lehigh ECE*, Since 09/2020, Topic: "Certifying and Enhancing the Reliability of NVM-based Processing-in-Memory Accelerator Design";

- Han Jiang, *Master at Lehigh ECE*, Since 12/2019, Topic: "AI-Assisted Medical Imaging".

Ph.D. Students (Graduated)

- Zihao Liu, *Ph.D. at FIU, Visiting Ph.D. at Lehigh*, 01/2016-07/2020;
  Ph.D. Thesis: "Machine vision, NOT Human Vision, Guided Compression towards Low-Latency and Robust Deep Learning Systems".
  First Employment: Research Scientist Alibaba DAMO Academy, CA.

- Tao Liu, *Ph.D. at FIU, Visiting Ph.D. at Lehigh*, 09/2016–07/2020;
  Ph.D. Thesis: "A System-level Perspective Towards Efficient, Reliable and Secured Neural Network Computing".
  First Employment: Tenure-Track Assistant Professor at Lawrence Technological University.

Undergraduate Students

- Lehigh ECE (2)-Casper Coleman (Female), Daniel Onyemelukwe;
  Project Title: "What's My Food? The Fridge Food Tracker", 09/2019-05/2020;

- FIU ECE (4)-Antonio Rubio (Hispanic), Geovanys Garcia (Hispanic), Thony Yan, Nicky Yan Liang;
  Project Title: "IMay, Machine Learning for the Everyday User", 09/2018-08/2019.

Awards of Advised Students

- Tao Liu, 1) Best Paper Award Nomination at ASP-DAC2018; 2) A. Richard Newton Young Student Fellow Award at DAC2017; 3) ACM Student Research Competition (SRC) Travel Award at ICCAD2017; 4) Graduate Travel Grants (twice) at HOST 2017/ HOST 2018.

- Qi Liu, 1) Best Paper Award Nomination at ASP-DAC2018; 2) Young Student Fellow Award at DAC2020.

- Nuo Xu, Young Student Fellow Award at DAC2020;

- Ruoyu Wang, Lehigh University Presidential Fellowship 09/2020-08/2021.

SERVICE

University

- ECE department Lehigh: Computer Engineering Curriculum Committee, 09/2019–05/2020.
- ECE department Lehigh: Faculty Search Committee, 09/2019–03/2020.

Professional

Conference Chairs, Organizers, Session Chairs

- Organizing Committee, DAC Early Career Workshop (Virtual), San Francisco, CA, July 2020;
- **General Chair**, 18th IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Miami, FL, July 2019;
- **Technical Program Committee (TPC) Chair**, 17th IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Hong Kong, China, July 2018;
- Financial Chair, 15th IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Pittsburgh, PA, 2016;
- Special Session Organizer/Chair, "Emerging Devices for Hardware Security: Fiction or Future", 15th IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Pittsburgh, PA, 2016;
- Poster Session Chair/Organizing Committee, IEEE International Symposium on Hardware Oriented Security and Trust (HOST), Washington, DC, 2017;
- Track Chair–VLSI for Machine Learning and AI, the 30th edition of the ACM Great Lakes Symposium on VLSI (GLSVLSI), Beijing, China, May 2020;
- Track Chair–Embedded System Architecture and Design, ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC), Tokyo, Japan, 2019;
- Track Chair–Emerging and Evolutionary Design, 30th IEEE International System-on-Chip Conference (SOCC), Munich, Germany, 2017;
- Session Chair, ACM/IEEE Design Automation Conference (DAC), San Francisco, CA 2018;
- Session Chair, IEEE International Conference on Computer-Aided Design (ICCAD), Austin, TX 2015, Irvine, CA, 2017 and San Diego, CA, 2018;
- Session Chair, ACM Great Lakes Symposium on VLSI (GLSVLSI), Banff, Alberta, Canada, 2017;
- Session Chair, ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC), Tokyo, Japan, 2017 and Jeju, Korea, 2018.

Technical Program Committee Member

- ACM/IEEE Design Automation Conference (DAC), 2019, 2020;
- ACM/IEEE ACM/IEEE Design, Automation & Test in Europe (DATE), 2020;
- ACM/IEEE International Conference on Computer Aided Design (ICCAD), 2017, 2018, 2019;

- IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP), 2019, 2020;
- IEEE Asia and South Pacific Design Automation Conference (ASP-DAC), 2017, 2018, 2019;
- IEEE International Conference on Computer Design (ICCD), 2017;
- ACM Great Lakes Symposium on VLSI (GLSVLSI), 2017, 2018, 2019, 2020;
- IEEE International Conference on Consumer Electronics (ICCE), 2017;
- IEEE International Conference on VLSI Design and 15th International Conference on Embedded Systems Design (VLSID), 2015-2017;
- IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2016-2018;
- IEEE International Conference on Network, Storage and Architecture (NAS), 2016;
- IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), 2016-2017.

Editorships

- Associate Editor, IEEE Circuits and Systems (CAS) Magazine, 2020-present
- Associate Editor, Neurocomputing, 2018-present;
- Guest Editor, IEEE Transactions on Circuits and Systems II (TCAS): Express Briefs, Special Issue, 2020-present;
- Guest Editor, ACM Journal on Emerging Technologies in Computing (JETC) Special Issue on New Trends in Nanoelectronic Device, Circuit and Architecture Design, 2019-present;

Reviewer

- Panelist, U.S. Department of Energy (DOE) Office of Science, 2016, 2018, 2019;
- Hong Kong Research Grant Council, 2020;
- Army Research Office (ARO) Research Award, 2017;
- IEEE Transactions on Neural Networks and Learning Systems (**TNNLS**);
- IEEE Transactions on Very Large Scale Integration (**TVLSI**) Systems;
- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**);
- IEEE Transactions on Multi-Scale Computing Systems (**TMSCS**);
- IEEE Transactions on Electron Devices (**TED**);
- ACM Journal on Emerging and Selected Topics in Circuits and Systems (**JETC**);
- ACM Transactions on Design Automation of Electronic Systems (**TODAES**);
- ACM Transactions on Embedded Computing Systems (**TECS**);
- IEEE Transactions on Computers (**TC**);

- IEEE Transactions on Communications (**TCOM**);
- IEEE Journal on Emerging and Selected Topics in Circuits and Systems (**JETCAS**);
- IEEE Transactions on Circuit and Systems II (**TCAS-II**);
- IEEE Transactions on Nanotechnology (**TNANO**);
- IEEE Design & Test of Computers (**D&T**);
- IEEE Transactions on Cyber-Physical Systems (**TCPS**);
- IEEE Embedded Systems Letters (**ESL**);
- IEEE Transactions on Wireless Communication (**TCOM**);
- IEEE Transactions on Sustainable Computing (**TSUSC**);
- Integration, the VLSI Journal;
- IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (**RTCSA**);
- IEEE International Test Conference (**ITC**);
- IEEE International Symposium on Circuits and Systems (**ISCAS**).